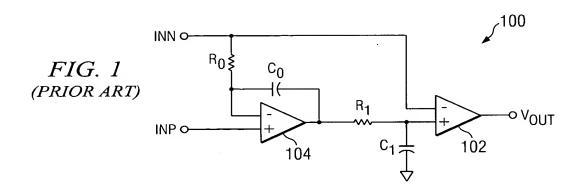
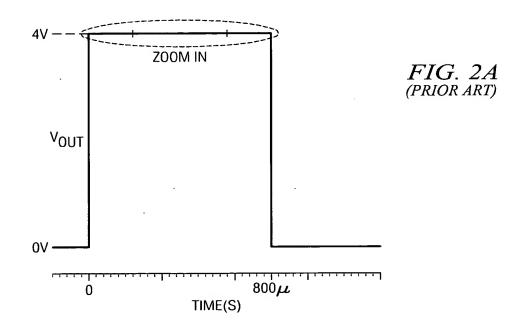
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1/3

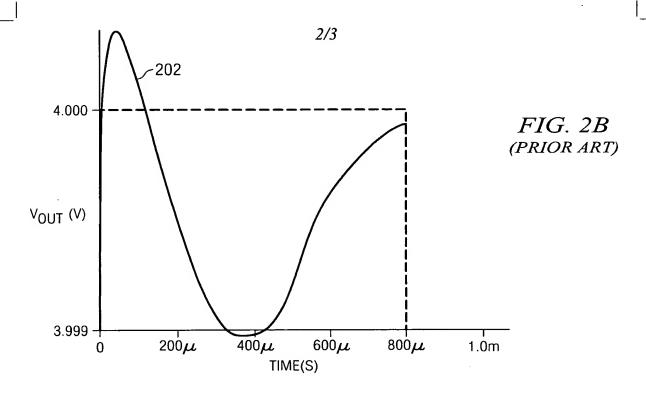
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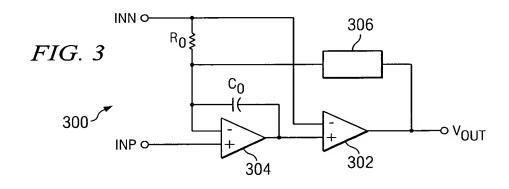


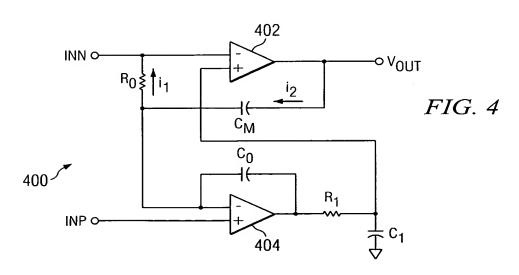
Method & Circuit for Reduced Settling
Time in an Amplifier
s): Rodney Burt et al.
lo.: 38880.7500 / TI-36094
R. Lee Fraley
602-382-6250
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Attorney: F
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3/3

